

Key Features

- Foundry proven memory cells
- Flexible aspect ratios through column and I/O multiplexing
- Separate input and output buses
- Flow Through, Pipelined Read options
- Write-through mode
- Duty-free clock cycle
- Optional ECC
- Advanced power reduction modes supported through sophisticated netlisting and layout tiling capabilities
- Flexible redundancy support: 1 or 2 dimensions. Laser or e-fuses
- Complete interface for EDA tools
- Allows routing over the array with higher metal layers
- Test multiplexing collar
- Complete test solution when used together with em-BIST test controllers

EMT Memory Compilers

EMT set of memory compilers include:

em-SRAM:

- SPSRAM: Single-Port(1R1W) Synchronous SRAM
- SPSRAMRD: Single-Port(1R1W) Synchronous SRAM with Redundancy
- DPSRAM: Dual-Port(2R2W) Synchronous SRAM
- DPSRAMRD: Dual-Port(2R2W) Synchronous SRAM with Redundancy
- SRFRAM: Multi-Port(1R1W, 2W1R, 2R2W) Synchronous Register File

em-DRAM:

- 1TRAMRD: Single-Port(1RW) Synchronous 1T1C embedded DRAM with Redundancy

em-ROM:

- DROM: Synchronous Diffusion based ROM
- VROM: Synchronous Via based ROM
- OTPROM: One Time Programmable ROM

Target processes

Current processes targeted include the following:

em-SRAM:

- TSMC 90nm G
- TSMC 90nm LP
- TSMC 65nm G
- TSMC 65nm LP
- Chartered 90nm G
- Chartered 90nm LP
- Chartered 65nm G
- Chartered 65nm LP

em-DRAM:

- TSMC 90nm G
- TSMC 90nm LP
- TSMC 65nm G
- TSMC 65nm LP

em-ROM:

- TSMC 90nm G
- TSMC 90nm LP
- Chartered 90nm G
- Chartered 90nm LP

Technical Specifications

Compiler Inputs

EMT memory compilers can be run through a Graphical User Interface (GUI), or in command mode.

The compiler user would provide the following parameters:

- Word Width
- Number of Words
- Multiplexer ratio (I/O and column)
- Minimum and Maximum voltage
- Minimum and Maximum temperature
- ECC (yes/no)
- Redundancy (yes/no)

Others input parameters may be required for specialized compilers

- Number of memory banks
- Power reduction modes
- Optional test modes
- Redundancy fuse sharing options
- Internal supply generator sharing for DRAM and Flash memories
- ROM bitmap

Compiler Editions

EMT Memory Compilers are typically available in two different editions:

- Preliminary Edition. Provides only front-end results based on simulation to provide accurate estimates to chip architects
- Final Edition. Provides both front-end and back-end outputs based on measured silicon data

Compiler Outputs

EMT memory compilers provide two main sets of outputs, front-end and back-end.

Front-end information is the set of views required by designers in the architecture and logic design phases. Front-end models are generated once the architecture and logic design is confirmed.

It includes the following views:

- Synopsys .LIB
- Synopsys .STAMP
- Verilog Behavioral
- Antenna LEF
- Datasheet Document

Back-End information is the set of views required to do the physical design of the target integrated circuit. It includes the following views:

- GDS II Layout
- LEF View
- SPICE LVS Netlist
- Gate Level Verilog Netlist

Requirements

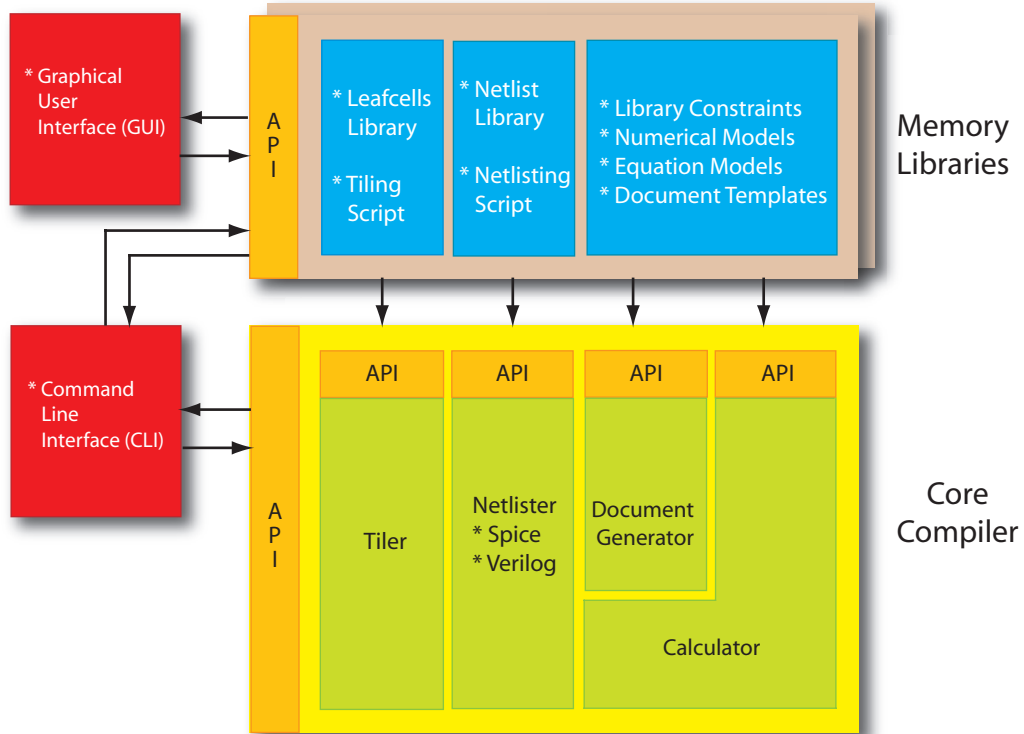
EMT's memory compilers are offered as a binary executable software program together with a library of technology specific data.

EMT currently supports the following Operating Systems:

- Red-Hat Linux on x86 compatible processor
- Sun Solaris on Sparc compatible processor

em-Kompiler

Core Compiler and Libraries



Full Test Solution: em-Kompiler and em-BIST

